

WE CLAIM:

1. A static logic circuit on a SOI substrate, comprising:

5

a pull-up network comprising a plurality of parallel connected MOS transistors with a first and second common node, wherein at least one of said plurality of parallel connected MOS transistors is a NMOS transistor and at least one of said plurality of parallel connected MOS transistors is a PMOS transistor;

10

a circuit supply voltage which is connected to said first common node of said pull-up network;

15

a pull-down network which is connected to said second common node of said pull-up network; and

an output node which is connected to said second common node of said pull-up network.

20

2. The static logic circuit of claim 1 wherein said pull-down network comprises a plurality of series connected MOS transistors connected to a circuit ground.

25

3. The static logic circuit of claim 2 wherein at least one of said plurality of series connected MOS transistors is a NMOS transistor and at least one of said plurality of series connected MOS transistors is a PMOS transistor.

30

4. The static logic circuit of claim 1 wherein at least one of said MOS transistors in said pull-up network has a gate tied to a floating substrate body.

5 5. The static logic circuit of claim 2 wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body.

TI-29319

6. A static logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel
5 connected MOS transistors with a first and second common
node, wherein at least one of said plurality of parallel
connected MOS transistors is a NMOS transistor and at least
one of said plurality of parallel connected MOS transistors
is a PMOS transistor;

10 a circuit ground which is connected to said first
common node of said pull-down network;

a pull-up network which is connected to said second
15 common node of said pull-down network; and

an output node which is connected to said second
common node of said pull-down network.

20 7. The static logic circuit of claim 6 wherein said pull-up
network comprises a plurality of series connected MOS
transistors connected to a circuit supply voltage.

8. The static logic circuit of claim 7 wherein at least one
25 of said plurality of series connected MOS transistors is a
NMOS transistor and at least one of said plurality of
series connected MOS transistors is a PMOS transistor.

9. The static logic circuit of claim 6 wherein at least one
30 of said MOS transistors in said pull-down network has a
gate tied to a floating substrate body.

10. The static logic circuit of claim 7 wherein at least one of said MOS transistors in said pull-up network has a gate tied to a floating substrate body.

TI-29319

11. A static logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel
connected PMOS transistors with a first and second common
5 node;

a circuit ground which is connected to said first
common node of said pull-down network;

10 a pull-up network which is connected to said second
common node of said pull-down network; and

an output node which is connected to said second
common node of said pull-down network.

15 12. The static logic circuit of claim 11 wherein said pull-
up network comprises a plurality of series connected NMOS
transistors connected to a circuit supply voltage.

20 13. The static logic circuit of claim 11 wherein at least
one of said MOS transistors in said pull-down network has a
gate tied to a floating substrate body.

25 14. The static logic circuit of claim 12 wherein at least
one of said MOS transistors in said pull-up network has a
gate tied to a floating substrate body.

15. A static logic circuit on a SOI substrate, comprising:

a pull-up network comprising a plurality of parallel
connected NMOS transistors with a first and second common
5 node;

a circuit supply voltage which is connected to said
first common node of said pull-up network;

10 a pull-down network which is connected to said second
common node of said pull-up network; and

an output node which is connected to said second
common node of said pull-up network.

15

16. The static logic circuit of claim 15 wherein said pull-
down network comprises a plurality of series connected PMOS
transistors connected to a circuit ground.

20 17. The static logic circuit of claim 15 wherein at least
one of said MOS transistors in said pull-up network has a
gate tied to a floating substrate body.

25 18. The static logic circuit of claim 16 wherein at least
one of said MOS transistors in said pull-down network has a
gate tied to a floating substrate body.